Tao XF, Hou YZ, Wang KD *et al.* GPP-based soft base station designing and optimization. JOURNAL OF COMPUTER SCIENCE AND TECHNOLOGY 28(3): 420–428 May 2013. DOI 10.1007/s11390-013-1343-3

# GPP-Based Soft Base Station Designing and Optimization

Xiao-Feng Tao[1] (陶小峰), Yan-Zhao Hou[1] (侯延昭), Kai-Dong Wang[1] (王凯栋), Hai-Yang He[1] (何海洋) and Y. Jay Guo[2] (郭英杰)

[1] *Key Lab of Universal Wireless Communications of Ministry of Education, Beijing University of Posts and Telecommunications, Beijing 100876, China*

[2] *CSIRO Information and Communication Technologies Centre, CnrVimiera & Pembroke Roads, Marsfield 2122, Australia*

E-mail: {taoxf, houyanzhao, kaitoon, hehaiyang}@bupt.edu.cn; Jay.Guo@csiro.au

Received October 5, 2012; revised March 14, 2013.

**Abstract** It is generally acknowledged that mobile communication base stations are composed of hardware components such as Field Programming Gate Array (FPGA), Digital Signal Processor (DSP), which promise reliable and fluent services for the mobile users. However, with the increasing demand for energy-efficiency, approaches of low power-consumption and high-flexibility are needed urgently. In this circumstance, General Purpose Processor (GPP) attracts people's attention for its low-cost and flexibility. Benefited from the development of modern GPP in multi-core, Single Instruction Multiple Data (SIMD) instructions, larger cache, etc., GPPs are capable of performing high-density digital processing. In this paper, we compare several software-defined radio (SDR) prototypes and propose the general architecture of GPP-based soft base stations. Then, the schematic design of resource allocation and algorithm optimization in soft base station implementation are studied. As an application example, a prototype of GPP-based soft base station referring to the 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) is realized and evaluated. To the best of our knowledge, it is the first Soft-LTE prototype ever reported. In the end, we evaluate the timing performance of the LTE soft base station and a packet loss ratio of less than 0.003 is obtained.

**Keywords** software radio, algorithm optimization, long term evolution

## 1 Introduction

In recent years, we have seen the emergence of a variety of wireless systems to support ever expanding services and applications. Meanwhile, energy consumed in wireless networks is increasing with the increasing number of base stations. According to [1], the base stations and backhaul networks of the cellular networks consume approximately 60 billion kWh per year, corresponding to roughly 0.33% of global electricity consumption. Although the architecture of wireless cells has been changing[2], the algorithm implementation stays the same as before, i.e., using hardware chips such as ASIC (Application Specific Integrated Circuit)/DSP (Digital Signal Processor)/FPGA (Field Programmable Gate Array). The function of ASIC chip is static and unchangeable. ASIC-based systems are still widely used in low-cost terminal devices. On the other hand, architectures based on FPGAs and DSPs are popular in the base stations. All those hardware chips promise a good performance and reliability, however, designing FPGAs and DSPs is a difficult task while the flexibility is also limited due to hardware components feature: different architectures cannot share the same code[3]. This would introduce high cost in both system maintenance and system upgrading. Thus, it is becoming important to realize wireless systems in a more energy-efficient and more flexible way. Mobile operators are facing a challenge to find new ways to resolve this problem①.

SDR (Software-Defined Radio) technology was proposed by Mitola to cope with above problems[4]. In SDR systems, all radio transmission, reception, signal generation, modulation/demodulation, timing control, coding and decoding are performed in software. In its infancy, SDR prototypes used DSPs/FPGAs to accomplish the baseband digital signal processing. Howe-

Regular Paper

This work is supported by the International Scientific and Technological Cooperation Program of China under Grant No. 2010DFA11060, the National Natural Science Foundation of China under Grant No. 61027003, the National Science and Technology Major Project of China under Grant No. 2012ZX03003008-003, and the Beijing Municipal Science and Technology Project under Grant No. D121100002112002.

The preliminary version of the paper was published in the proceedings of CHINACOM 2012.

①China Mobile Research Institute. C-RAN: The road towards green RAN. http://labs.chinamobile.com/cran/, October 2012.

©2013 Springer Science + Business Media, LLC & Science Press, China

ver, benefiting from the development of modern GPP (General Purpose Processor) technologies, GPPs are getting better to accomplish computing-intense jobs in modern high-speed wireless communication systems and break through the limitation mentioned above. Technology evolution in areas such as multi-core, SIMD (Single Instruction Multiple Data), large on-chip caches, low latency off-chip system memory and high-speed I/O enabled GPP to process high speed digital signal flow in wireless base station systems.

So far, several SDR prototypes have been introduced. A commercially available software base station that could support CDMA (Code Division Multiple Access) and GSM (Global System of Mobile Communication) simultaneously was developed by Vanu, Inc.[5] Eruecom's project — Wireless3G4Free implemented the 3GPP (3rd Generation Partnership Project) UMTS (Universal Mobile Telecommunications System) high chip rate (3.84 Mchip/s) access stratum protocols with an IP-based interconnection with off-the-shelf 802.11 WLAN (Wireless Local Area Network) solutions②. Furthermore, OpenAirInterface[6] provides an experimental open-source real-time hardware and software prototype for experimentation in wireless networks. SDR system in [7] seamlessly integrates four standards and their frequency bands and modulation modes, i.e., IS-95, GSM, DCS1800 and TACS (Total Access Communications System), which realized wireless voice communications under the four standards. Prototypes mentioned above have limited performance and their processing capability is insufficient for future high-speed wireless protocols. WARP (Wireless Open Access Research Platform)[8-9], developed by Rice University, is a scalable and programmable wireless prototype. The primary communication processor used in it is an Xilinx Viretex-4 FPGA and an embedded PowerPC processor in the FPGA provides a complete embedded programming environment for MAC (Media Access Control) and network layer design. That means, FPGA for physical layer and CPU for higher layer. PicoArray is an SDR prototype based on fine-grained reconfigurable FPGA-like computation fabrics[10]. One of the major drawbacks of the fine-grain computation fabrics is the high communication cost of data shuffling within the computation fabrics. GNU Radio③, is another well-known SDR prototypes, in which wireless physical layer processing is done entirely in software based on GPP. Although it aids in reprogramming using simple high level programming languages, they often fail to meet the protocol timing requirement for modern wireless protocols such as 802.16 because of a combination of I/O throughput and post-processing using commercial CPUs. Its peak rate is only hundreds of Kbps. A TD-SCDMA (Time Division-Synchronous Code Division Multiple Access) system based on common PCs was designed in [11], which has a data rate of 64 Kbps. SODA[12] provides a multi-processor architecture using optimized SIMD operations for digital processing. It can meet the computational requirements for 2 Mbps W-CDMA (Wideband CDMA) and 24 Mbps 802.11a by four DSP processors, but a single-chip structure is more appropriate for embedded scenarios. Sora, proposed by MSRA (Microsoft Research Asia)[13], allows researchers to implement and debug high-speed wireless protocols entirely in software with familiar programming environment, e.g., C/C++ language, and conduct real over-the-air experiments. Its peak data rate can be around 30 Mbps. Currently, Sora provides solutions to the WLAN networks like 802.11a/b, which are intended for indoor use with stationary terminals and have relatively simple MAC protocols, and yet it is still a big challenge for Sora to run the next generation high speed protocol. Besides above SDR prototypes, some novel wireless technologies are emerging. In [14], developers simulated the SDR environment using GPU (Graphics Processing Unit) to realize some algorithms in wireless baseband, interestingly but regretfully, they only evaluated the basic processing such as FFT (Fast Fourier Transform), and IIR (Infinite Impulse Response). GPP-based SDR front-end for WLAN was also designed[15]. A low-complexity compensation scheme for timing synchronization error in GPP-SDR was also proposed[16].

The GPP-based SDR prototypes and technologies mentioned above demonstrate that the GPP has the capability to process wireless high-speed information flow with the evolvement of GPP technologies. However, the next generation wireless systems take on features of higher data rate (> 100 Mbps), wider bandwidth (> 20 MHz), lower latency (<10 ms), and yet the timing performance in GPP-based wireless prototypes has not been mentioned before. For this reason, we present a basic architecture of GPP-based soft base stations in this paper, and propose feasible solutions to cope with high data throughput and timing problems in current GPP environment. To demonstrate our methods, we further design a prototype of soft base station, referring to 3 GPP LTE (Long Term Evolution) standard. Through our test, we prove that GPP-based soft base stations are able to bear high-speed wireless protocols and provide a more flexible way in system control and maintenance.

②http://www.wireless3g4free.com/, March 2013.

③http://gnuradio.org/redmine/, March 2013.

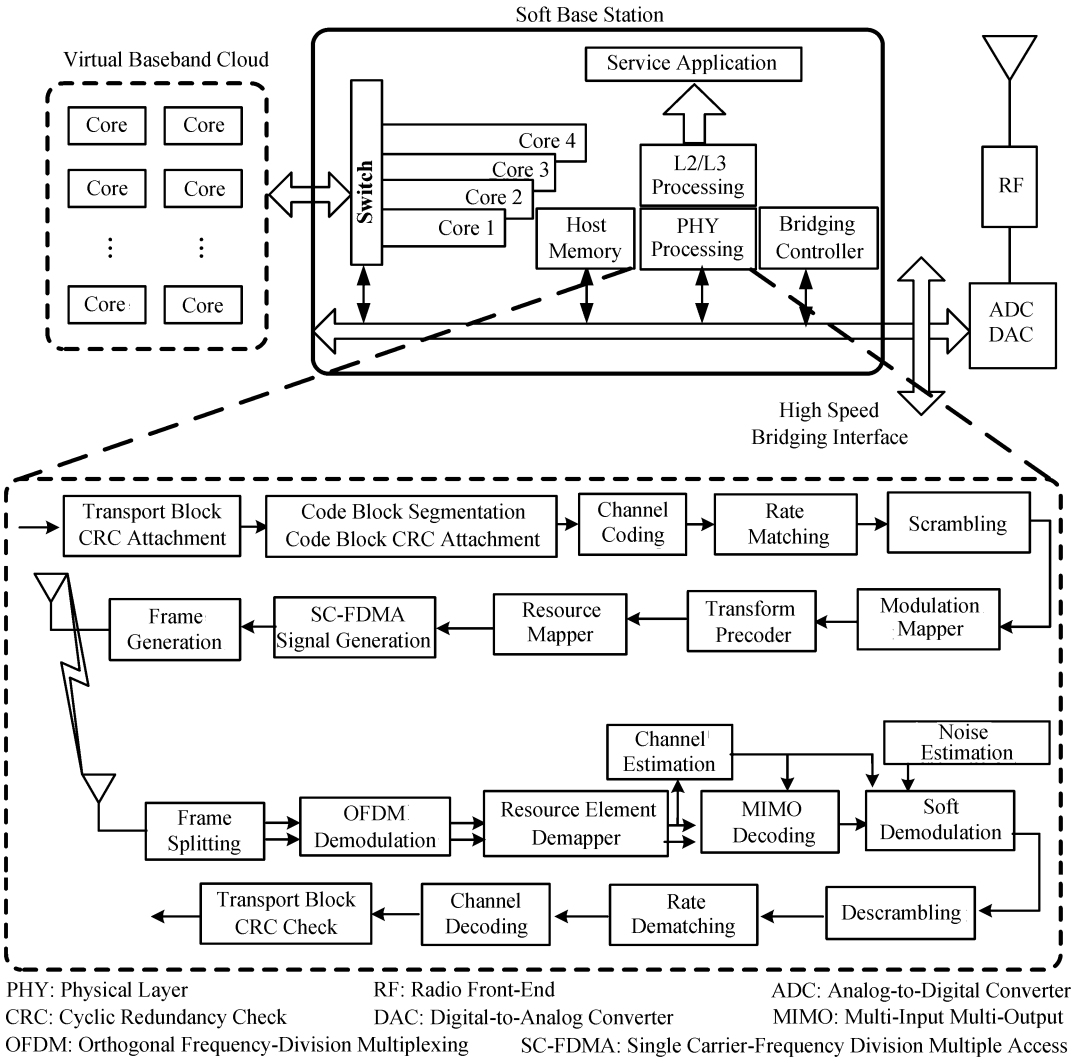


Fig.1. Typical software radio architecture.

Key features of the next generation wireless systems including higher data rate, wider bandwidth and lower latency, pose some challenges to soft base stations. This paper is organized as follows. Section 2 gives a brief description of the soft base station systems and the obstacles in soft base station design. The resource allocation and algorithm optimization, as well as the timing evaluation are described in Section 3. In Section 4, the prototype of LTE soft base station is shown as an application example. Finally, Section 5 gives the conclusions.

## 2 GPP-Based Soft Base Station Primary

### 2.1 System Description

A typical base station system consists of RF (radio front-end) modules, AD/DA converters, bridging interface, baseband processing modules and L2/L3 processing modules. In GPP-based soft base station, RF and AD/DA modules stay the same compared with traditional hardware base stations except baseband processing. L2/L3 processing is replaced by software library which can support multiple protocols, and the bridging interface is also changed based on the operating system. As shown in Fig.1, an example of 3 GPP LTE signal receiving procedure is given to explain the function of each block. Analog signals are received by RF module, and then they are digitalized by AD converters into digital signal flow. The bridging interface, such as PCIe (Peripheral Component Interconnect Express) bus/USB (Universal Serial Bus) 3.0, transfers the digital signal flow into the host memory. Baseband signal processing is performed inside GPP as well as L2/L3 processing under a proper mapping on different cores. Then upper layer interface distributes the signals to different service applications. Given that baseband processing is facilitated in GPPs, optimization schemes are

also needed to be considered in order to guarantee real-time high-speed communication as well as fidelity.

Cloud computing can be utilized to enhance the GPP processing ability. Multiple geographically distributed cores can be concentrated into a virtual baseband pool. Limited by the length of this paper, we here mainly focus on the GPP core resource allocation and algorithm optimization.

### 2.2 Obstacles in Implementation

Since our approach is completely different from that of the traditional base stations, currently there still exist many obstacles in soft base station design.

#### *2.2.1 Computation Requirements*

From software point of view, the most important issue in GPP-based soft base stations is to realize the time-sharp wireless communication baseband processing using software. As the development of modern wireless protocols, the data throughput and computation requirements are getting higher. Thus, a well-written software/algorithm is required to satisfy the substantial need for computing. We can get the different round trip time of different wireless protocols④∼⑥. Specially, LTE baseband processing needs to be done within 5ms in order to support a higher wireless speed.

#### *2.2.2 Timing Requirements*

Both 4 G and Beyond 4 G systems support TDD (Time Division Duplex) and FDD (Frequency Division Duplex) mode. Especially in TDD system, uplink/downlink switch is determined by a global clock in the base station. As for a GPP-based soft base station, we have two clock sources: one inside the GPP and the other inside the RF module. With respect to the instruction transmission delay from GPP cores to RF module, controlling the uplink/downlink switch is a key challenge.

## 3 Resource Allocation and Algorithm Optimization

### 3.1 Resource Allocation

Take 3 GPP LTE baseband processing as an example (Fig.1), we can see that physical layer processing typically contains several functional blocks in a feed-forward pipeline. These blocks differ in processing speed and input/output data rates. Usually, a block is ready to run only if the previous block provides sufficient data. Therefore, the key issue would be how to schedule each block on multiple cores.

Traditionally, the scheduling schemes in CPU are divided into two categories: static scheduling and dynamic scheduling. In scheme selection, we should take the wireless communication features into consideration. Wireless communication is an ongoing process and the data stream has a strong dependency. For example, in turbo coding, the output bits depend on four preceding bits in the stream. If we use dynamic scheduling, the overhead spent on synchronization and data exchanging would be extremely high. What is more, high speed wireless communications are often characterized by large size physical layer blocks (5 504 bytes in LTE). Dynamic core allocation will cause a high inter-core communication overhead.

Thus, in soft base stations, we use static scheduling to allocate computing resources. High complexity function blocks, such as turbo decoding, can occupy one whole CPU core to guarantee the real-time demand. Between different cores, an FIFO would be used to synchronize the data stream. Thus, low overhead spent on inter-core exchange and synchronization will be introduced.

### 3.2 Algorithm Optimization

#### *3.2.1 Optimization Methodology*

Thanks to the development of modern GPP technologies, such as multi-core, SIMD instructions, large on-chip caches, high speed I/O, the processing ability of current commercial GPP is greatly enhanced. The theoretical processing gain ($G$) and processing ability ($A$) of GPPs can be calculated by the following equations:

$$G = N \times \lambda \times \frac{W_{\mathrm{I}}}{W_{\mathrm{D}}},$$

$$A = f \times N \times \lambda \times \frac{W_{\mathrm{I}}}{W_{\mathrm{GPP}}},$$

where $f$ is the frequency of GPP, $N$ is the number of processing cores inside GPP, $\lambda$ is the number of hyper thread per core, $W_{\mathrm{I}}$ is the width of instructions, $W_{\mathrm{D}}$ is the width of signal data and $W_{\mathrm{GPP}}$ is the width of GPP. Take Intel i7 3.4 GHz/6 cores/32 bits-width CPU for example, we utilize multithread and 128-bit instruction to process 16-bit data, which can obtain a theoretical gain of 96 times and a processing ability of 163.2 GOPS

④Evolved universal terrestrial radio access. 3 GPP TS 36.201. http://www.3gpp.org/ftp/Specs/html-info/36201.htm, March 2013.

⑤Services and service capabilities. 3GPP TS 22.105. http://www.3gpp.org/ftp/Specs/html-info/22105.htm, March 2013.

⑥Physical layer aspects for evolved universal terrestrial radio access. 3GPP TR 25.814. http://www.3gpp.org/ftp/specs/html-INFO/25814.htm, March 2013.

(giga operations per second). We can see that current commercial GPPs have an equal processing capability compared with traditional hardware computing units and can meet a high level computation requirements of base station physical layer.

Using multi-core and introducing multi-thread can guarantee the processing requirement of GPPs, however, data traffic could be so heavy that it will cause a high overhead spent on data transfer between different cores (Table 1)[17]. Thus we should think over how to accommodate baseband function blocks into multi-core environment to improve the efficiency of GPPs. On the other hand, appropriate algorithm should also be well optimized in single core/function block w.r.t both reliability and efficiency, taking advantage of SIMD, large on-chip cache, etc.

**Table 1.** Data Throughput in Physical Layer Processing

| Module | Throughput (bps) |
|---|---|
| EDGE (Enhanced Data Rates for GSM Evoluation) | 96.00 K |
| HSPA (High Speed Packet Access) | 640.00 M |
| LTE (Long Term Evolution) | 1.28 G |

We use the following model to describe our target: the whole baseband signal processing blocks in GPP-based soft base stations can be realized by multi-core or multi-thread. We use $M_i$ to indicate the processing unit (core/thread) in GPP, and $N_i$ to indicate the number of jobs processed by the same unit $M_i$. Theoretically, our target is to obtain the optimal value of the follow expression:

$$\min_{M_i}\Big(\max_{j\in M_i}\sum_{j=1}^{N_i} CT_j + ET_j\Big),$$
$$\text{s.t. } CT_j,\ ET_j \geqslant 0, \quad j=1,\ldots,N, \tag{1}$$

where $CT_j$ means the communication time of job $j$ and $ET_j$ means the executing time of job $j$.

From (1), we can see that efficient resource allocation will reduce the communication overhead among multi-core/thread ($CT_j$), and algorithm optimization will reduce the execute time of the baseband processing blocks ($ET_j$). Thus, from the view of implementation, we focus on the schematic design of resource allocation and algorithm optimization.

### 3.2.2 SIMD Processing

In traditional hardware wireless communication systems, the SIMD instructions are also used which separates the register file into clusters. However, in most traditional commercial solutions, SIMD width is conservatively limited from 4 bits to 8 bits, due to data array alignment difficulties in general purpose DSP computations[12]. This situation is getting optimistic in GPP application. As far as we know, most GPPs can support wide SIMD instructions now, such as MMX (Multi Media eXtension), SSE (Streaming SIMD Extension), SSE2, 3DNow, and so on. SIMD allows us to do logical operations among eight 128-bit registers, which means that we can handle 128-bit data in one single instruction cycle.

For channel decoding, we use the log-map algorithm proposed by [18]. In the iteration of LLR (log-likelihood ratio) computing, there are three parameters to be calculated: $\gamma$, $\alpha$, $\beta$, where $\gamma$ is the branch transition probability, $\alpha$ is the forward recursion, and $\beta$ is the backward recursion.

In Table 2, we can see that after using SSE instructions (Fig.2), we can obtain a variety of gain in turbo decoding. By doing this, we make sure that the time consumption by turbo decoding meets the real-time demand.

**Table 2.** Processing Gain by SIMD Processing in Turbo Decoding

| Parameter | Theoretical Value | Realization Value | Gain | Time Consumption (ms) |
|---|---|---|---|---|
| $\gamma$ | 66 240 | 11 730 | 5.6 | $< 0.2$ |
| $\alpha$ | 220 800 | 104 652 | 2.1 | $< 0.6$ |
| $\beta$ | 220 800 | 104 652 | 2.1 | $< 0.6$ |

```
GammaStart:
    pshufd xmm0, [eax], 0xe4;
    pshufd xmm1, [ecx], 0xe4;
    pshufd xmm4, [exa + 5 520], 0xe4;
    paddsh xmm0, xmm1; //sys(15:0) + exti(15:0)
    movdqa [ecx], xmm0;
    pxor xmm0, xmm7; //(− sys − esti)
    paddsb xmm0, CharOne;
    pshufd xmm1, xmm0, 0xe4; //(− sys − esti)
    psubsb xmm0, xmm4; //(− sys − esti − code),
    paddsb xmm1, xmm4; //(− sys − esti + code);
    pshufd xmm2, xmm1, 0xe4; //(− sys − esti + code)
    pshufd xmm3, xmm0, 0xe4; //*0sys − esti − code)
    pxor xmm2, xmm7; //(sys + esti − code)
    paddsh xmm2, CharOne;
    pxor xmm3, xmm7; //(sys + esti + code)
    paddsb xmm3, CharOne;
```

Fig.2. Part of the SSE codes.

### 3.2.3 Multi-Thread Parallel Processing

As we discussed in Section 2, the wireless physical layer is a pipeline composed of different functional blocks. This feature allows us to facilitate the parallel processing using multi-thread. Given that inter-core

communication will result in a large overhead in high-speed wireless protocols, we use two concurrent threads in the same core.

Take synchronization as an example, we use the low-complexity synchronization algorithm proposed by [19]. Based on our research, time spent on synchronization costs almost 50% of the whole time spent on the physical layer processing. Given that signals received by soft base station are firstly stored in an FIFO pipe, we can parallel the synchronization block with the other physical layer processing blocks, and place them into two parallel threads, as shown in Fig.3. In this way, we can reduce the whole time by nearly 50%.

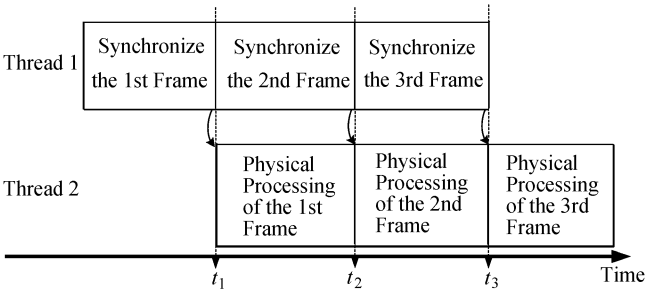


Fig.3. Parallel processing model in multi-core.

### *3.2.4 Look-Up Table Processing*

LUTs (look-up tables) are widely used in hardware designing. Its fundamental idea is to convert mathematical algorithm to find the answer in a pre-created table. Gain by this in software is particularly evident. It largely reduces the time spent on calling sub-functions.

As we discussed earlier, the capacity of high-speed cache memory has grown even larger. Contemporary modern CPUs, such as Intel Core 2, usually have megabytes of L2 cache with a low (10∼20 cycles) access latency. Thus, we can greatly reduce the processing requirements by LUTs which are pre-stored in the cache.

Actually, more than half of the physical layer blocks can indeed be optimized by LUTs. Fig.4 shows the gain we obtained in CRC and DFT algorithms through LUTs. Large usage of LUTs makes sure that the processing time delay meets the high-speed protocol's demand.

## 3.3 Timing Performance

In this subsection, we mainly evaluate the timing performance in the TD-LTE system. Traditionally, RS (reference signal) is utilized to synchronize the clock frequency in order to tell UE (user equipment) when to receive and when to transmit wireless signals.

As shown in Fig.5, $t_{\text{trans}}$ represents the time delay

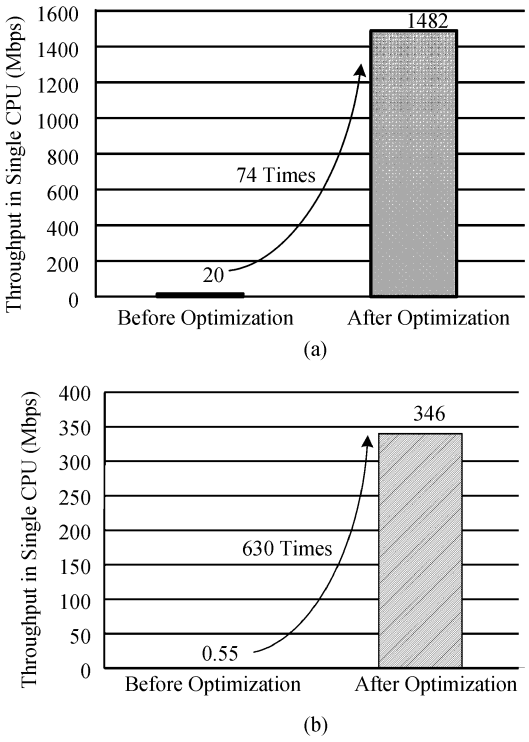


Fig.4. (a) CRC processing gain by LUTs. (b). DFT processing gain by LUTs.

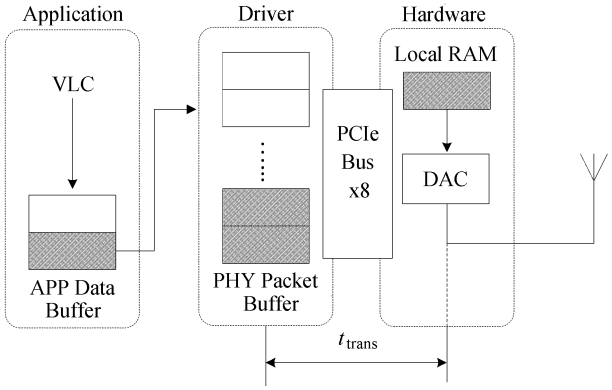


Fig.5. Transmitter illustration.

between transmit command execution and signal transmission beginning. Since we use PCIe x8 to transfer data and instructions between CPU memory and local RAM on the RF side, there exists a tiny delay jitter along the transfer link.

Here we try to use a round-trip method (Fig.6) to get the delay jitter which can be equal to:

$$T_{\text{jitter}} = (T_2 - T_1 - T_{\text{tx}})/2,$$

where $T_{\text{tx}}$ represents the time spent on transmitting the samples; the RF sample rate is 44 MHz, thus $T_{\text{tx}}$ equals to the number of samples divided by $44 \times 10^6$. Fig.7 shows the delay jitter performance.

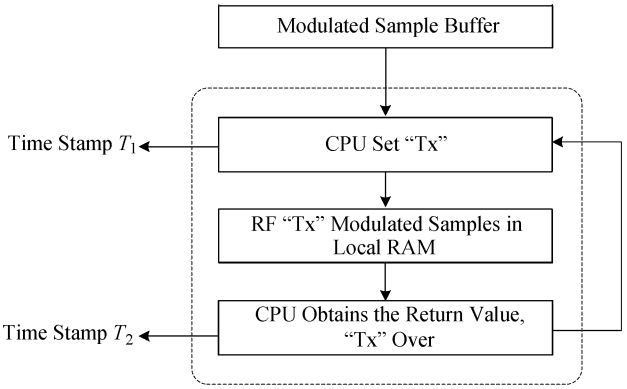


Fig.6. Instruction delay testing procedure.

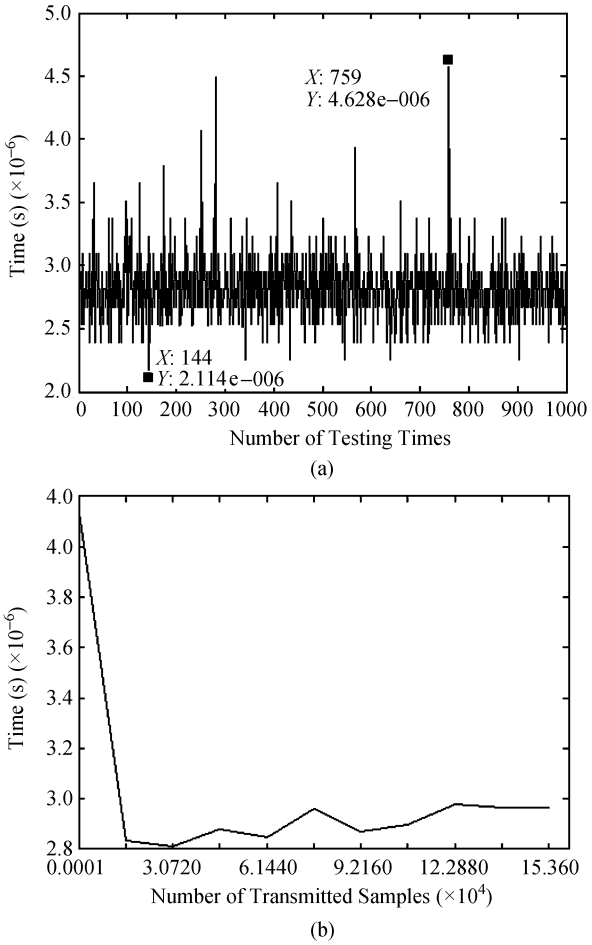


Fig.7. (a) Instruction delay performance when "Tx" 153 600 samples. (b) Instruction delay performance when "Tx" different numbers of samples.

From Fig.7(a) we can see that the maximum delay jitter is 2.5 $\mu$s, meanwhile, due to more than 15 360 samples would be transmitted in an ordinary wireless service, we can see that the average delay equals to 2.9 $\mu$s in Fig.7(b). Under our test (RF sampling rate equals to 44 M), a delay jitter of 2.5 $\mu$s means a time shift jitter of 110 samples which is less than the length of CP (cyclic prefix) and we can compensate this time shift by CP. Thus we take above time delay into account when designing the transmitter and receiver. By doing this, the packet loss ratio is reduced to less than 0.003.

## 4 Case Study and Results

Based on our previous research, we design a GPP-based prototype which refers to 3 GPP LTE protocol⑦. It achieves part of the functions in soft base stations and can realize real-time communication.

Our prototype employs Intel i7 CPU for baseband signal processing. The CPU has four cores of 3.2 GHz and also supports hyper thread. For the hardware, PCIe x8 is adopted which has a maximum throughput of 16 Gbps. The ADC/DAC has a resolution of 16 bits and the signal is represented by 32 bits because of the quadrature sampling. At the physical layer, an LTE PUSCH&PDSCH link is designed for the trial system. Table 3 lists the parameters we use in the prototype. It is noted that we use 44 MHz instead of the theoretical value of 30.72 MHz as the sampling rate because of the hardware limitation. At the receiver side, two FIFO pools are used to cache signals and parallel the synchronization with other physical layer processing blocks as we discussed before. At the application layer, we use VLC Media Player to show the video we received.

**Table 3.** Parameters of Prototype System

| Parameters | Settings |
|---|---|
| AD/DA converter | 16 bits |
| Bandwidth | 20 MHz |
| Subcarrier spacing | 15 KHz |
| Sampling frequency | 30.72 MHz |
| FFT size | 2 048 |
| CP size | 160 (1st symbol) |
| | 144 (2nd∼7th symbol) |
| Frame length | 10 ms |
| Subframe length | 0.5 ms |
| Channelcoding rate | 3/4 |
| Modulation | 16 QAM |
| Peak data rate | 45 Mbps |

In the prototype, we use two cores out of the four as soft base station processing cores, thus other applications can run on the other two cores. We allocate different processing resources to each function block (Fig.1) based on its processing demand.

As seen in Table 3, samples are presented in 32-bit wide including 16-bit I branch and 16-bit Q branch

⑦Evolved universal terrestrial radio access. 3 GPP TS 36.201. http://www.3gpp.org/ftp/Specs/html-info/36201.htm, March 2013.

separately. The sampling rate is 30.72 MHz, thus we can get 983.04 Mbps digital signal stream which can be transferred by PCIe bus. By optimization methods we discussed above, we can obtain a peak data rate of 45 Mbps. One LTE frame is captured in the air and the real-time frame analysis results are showed in Fig.8 and Fig.9.

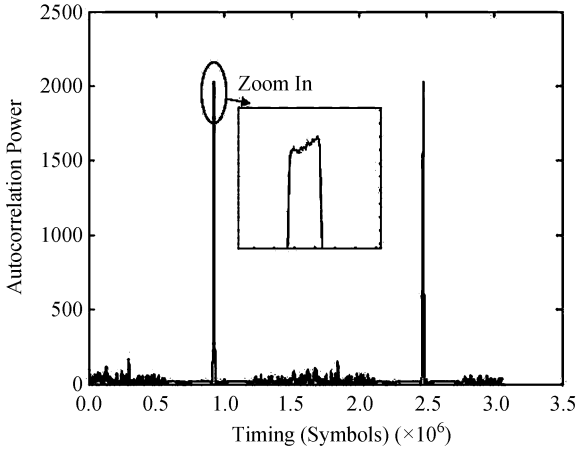


Fig.8. Synchronization result.

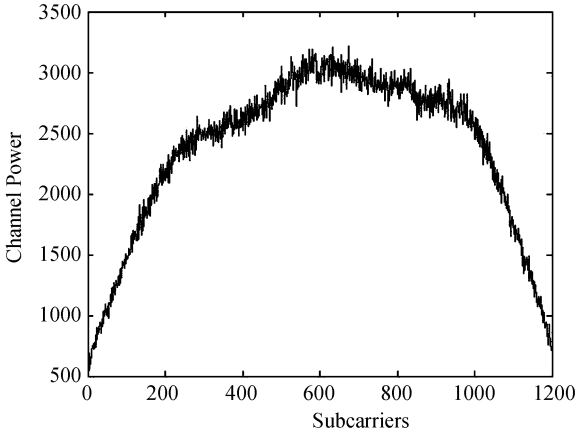


Fig.9. Channel estimation result.

Fig.8 shows the synchronization performance at the receiver. The estimated error of frame start is controlled less than 60 time slots (within the CP) so that the frame can be decoded correctly. Synchronization is a time-consuming job, and we need a parallel thread to handle it while guarantee its performance as discussed before.

From Fig.9 we can see that good channel estimation results are obtained and most power is concentrated in the center of our designed 1 200 subcarriers. However, more complex algorithms should be used in soft base stations in order to improve the system robustness against fading channels, which will be done in our future work.

## 5 Conclusions

In this paper, we proposed the typical architecture of GPP-based soft base stations. Then we mainly discussed the computing resource allocation and algorithm optimization in soft base stations. Based on proper core allocation and optimization schemes, a prototype for 3 GPP LTE was implemented, which could reach a peak data rate of 45 Mbps. Moreover, we pointed out that there will be a degradation of performance because of the clock jitter in the TDD SDR. In our prototype, we obtained the clock delay by a round trip method and compensated it. Through this way, the timing performance as well as synchronization and block error rate (BLER) results were evaluated. Test results showed that it could satisfy the demand for future high-speed wireless communications.

For our future work, we are planning to complete the soft-LTE base station prototype to include the MAC layer. Some key problems such as interfaces among GPPs, coordinated resource allocation schemes, are needed to be addressed. From the view of research, coordinated multi-point processing and centralized baseband processing would be efficient ways to improve spectrum efficiency and energy efficiency.

**Acknowledgement** The authors would like to thank the anonymous reviewers and the editors for their valuable comments and suggestions to improve the paper's quality.

## References

[1] Fettweis G, Zimmermann E. ICT energy consumption — Trends and challenges. In *Proc. the 11th Int. Symp. Wireless Personal Multimedia Commun.*, September 2008, pp.4-6.

[2] Tao X F, Xu X D, Cui Q M. An overview of cooperative communications. *IEEE Communication Magazine*, 2012, 50(6): 65-71.

[3] Gudaitis M S, Hinman R D. Tactical software radio concept. In *Proc. MILCOM 1997*, November 1997, Vol.3, pp.1207-1211.

[4] Mitola J. Software radio architecture: A mathematical perspective. *IEEE Journal on Selected Areas in Communications*, 1999, 17(4): 514-538.

[5] Muir S, Yedetore J, Stich L, Chapin J. Integration of SDR cellular basestations into military telephone networks. In *Proc. 2007 Military Communications Conference*, October 2007, pp.1-7.

[6] Kaltenberger F, Ghaffar R, Knopp R, Anouar H, Bonnet C. Design and implementation of a single-frequency mesh network using OpenAirInterface. *EURASIP Journal on Wireless Communications and Networking,* 2010, 2010: Article No.19.

[7] Zhao S J, Shen C, Su X, Yao Y. Architecture of a software radio system based on cluster of workstations. In *Proc. IEEE TENCON 2003*, October 2003, Vol.4, pp.1439-1444.

[8] Murphy P, Hunter C, Sabharwal A. Design of a cooperative OFDM transceiver. In *Proc. the 43th Asilomar Conference on Signals, Systems and Computers*, November 2009, pp.1263-1267.

[9] Hunter C, Camp J, Murphy P, Sabharwal A, Dick C. A flexible framework for wireless medium access protocols. In *Proc. the 40th Asilomar Conference on Signals, Systems and Computers*, November 2006, pp.2046-2050.
[10] Pulley D, Baines R. Software defined baseband processing for 3G base stations. In *Proc. the 4th International Conference on 3G Mobile Communication Technologies*, June 2003, pp.123-127.
[11] Huang L, Zheng K, Wang X Y, Decarreau G. Timing performance analysis in an open software radio system. In *Proc. the 1st International Conference on Communications and Networking in China*, October 2006, pp.1-5.
[12] Lin Y, Lee H, Woh M *et al.* Soda: A low-power architecture for software radio. In *Proc. the 33rd International Symposium on Computer Architecture*, June 2006, pp.89-101.
[13] Tan K, Zhang J S, Fang J, He L, Ye Y S, Wang S, Zhang Y G, Wu H T, Wang W, Voelker G M. Sora: High performance software radio using general purpose multi-core processors. *Communications of the ACM*, 2011, 54(1): 99-107.
[14] Horrein P H, Hennebert C, Pétrot F. Adapting a SDR environment to GPU architectures. In *Proc. SDR11-WInnComm-Europe Conference*, June 2011, pp.143-149.
[15] Schiphorst R, Hoeksema F, Arkesteijn V, Slump K, Klumperink E, Nauta B. A GPP-based software-defined radio front-end for WLAN standards. In *Proc. IEEE Benelux Signal Processing Symposium*, April 2004, pp.203-206.
[16] Tao X F, Wang K D, He H Y, Hou Y Z, Han J. A compensation scheme for timing synchronization error in GPP-SDR LTE system. In *Proc. the 1st International Conference on Communications in China*, August 2012, pp.339-344.
[17] Lin Y H, Shao L, Zhu Z B, Wang Q H, Sabhikhi R K. Wireless network cloud: Architecture and system requirements. *IBM Journal of Research and Development*, 2010, 54(1): 38-49.
[18] Erfanian J, Pasupathy S, Gulak G. Reduced complexity symbol detectors with parallel structure for ISI channels. *IEEE Transactions on Communications*, 1994, 42(234): 1661-1671.
[19] Schmidl T M, Cox D C. Robust frequency and timing synchronization for OFDM. *IEEE Transactions on Communications,* 1997, 45(12): 1613- 1621.

**Xiao-Feng Tao** received his B.S. degree in electrical engineering from Xi'an Jiaotong University, China, in 1993, and M.S.E.E. and Ph.D. degrees in telecommunication engineering from Beijing University of Posts and Telecommunications (BUPT) in 1999 and 2002, respectively. He was a visiting professor at Stanford University from 2009 to 2011, chief architect of Chinese National FuTURE 4G TDD working group from 2003 to 2006 and established 4G TDD CoMP trial network in 2006. He is currently a professor at BUPT, Fellow of IET (The Institution of Engineering and Technology), the inventor or co-inventor of 50 patents, the author or co-author of 120 papers, in 4 G and beyond 4 G.

**Yan-Zhao Hou** is currently a Ph.D. candidate in communication engineering in Beijing University of Posts and Telecommunications (BUPT). His research interests include software-defined radio technology and key technologies in physical layer in the next generation wireless communications.

**Kai-Dong Wang** is currently pursuing the M.S. degree of communication engineering in Wireless Technology Innovation Institute and Key Laboratory of Universal Wireless Communications (Ministry of Education), BUPT. His research interests include software-defined radio based on GPPs, wireless and satellite communications.

**Hai-Yang He** is currently working toward the M.S. degree of communication engineering in Wireless Technology Innovation Institute and Key Laboratory of Universal Wireless Communications (Ministry of Education), BUPT. His research specializes in software-defined radio based on GPPs, and physical layer technologies for 4G.

**Y. Jay Guo** is the research director of the Smart and Secure Infrastructure portfolio (Theme) in CSIRO, Australia, which covers broadband networks and services, smart home and communities, and cyber-physical security. Prof Guo is a leading researcher in antennas and propagation, gigabit wireless communications systems and wireless positioning. He is the fellow of IET, an adjunct professor at the University of New South Wales, Macquarie University and University of Canberra, and a guest professor at the Chinese Academy of Sciences and Shanghai Jiaotong University. He has published over 200 research papers including 84 journal papers and 3 scholarly books, and holds 18 patents.