Wang W, Hu Y, Han YH *et al.* Leakage current optimization techniques during test based on don't care bits assignment. JOURNAL OF COMPUTER SCIENCE AND TECHNOLOGY 22(5): 673∼680 Sept. 2007

Leakage Current Optimization Techniques During Test Based on Don't Care Bits Assignment

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Received June 16, 2005; revised May 8, 2007.

Abstract It is a well-known fact that test power consumption may exceed that during functional operation. Leakage power dissipation caused by leakage current in Complementary Metal-Oxide-Semiconductor (CMOS) circuits during test has become a significant part of the total power dissipation. Hence, it is important to reduce leakage power to prolong battery life in portable systems which employ periodic self-test, to increase test reliability and to reduce test cost. This paper analyzes leakage current and presents a kind of leakage current simulator based on the transistor stacking effect. Using it, we propose techniques based on don't care bits (denoted by Xs) in test vectors to optimize leakage current in integrated circuit (IC) test by genetic algorithm. The techniques identify a set of don't care inputs in given test vectors and reassign specified logic values to the X inputs by the genetic algorithm to get minimum leakage vector (MLV). Experimental results indicate that the techniques can effectually optimize leakage current of combinational circuits and sequential circuits during test while maintaining high fault coverage.

Keywords leakage current, don't care bits, minimum leakage vector, leakage power

1 Introduction

It is well known that power dissipation during test mode can be significantly higher than that during functional mode. Sometimes, the test power could be twice as high as the power consumed during the normal mode[1]. Furthermore, the proportion of the leakage current power to the total power increases rapidly. Consequently, as leakage current becomes a big contributor to test power consumption, leakage current optimization in test will be a very important research topic.

In recent years, dynamic power consumption is a dominant component of total power dissipation during test. A considerable amount of effort has been expended in reducing dynamic power or other test cost[2∼11]. However, as technology scales down below 0.13 micron, the absolute and the relative contribution of leakage power to the total system power during test is expected to further increase because of the exponential increase in leakage current, setting leakage power consumption on the path to dominating the total power used by the CPU[12]. Thus, reducing leakage current during test is also becoming an increasingly important issue. Especially to Very Deep Sub-Micron (VDSM) IC (integrated circuit) during test, large leakage current would cause crosstalk noise and functional failures etc. Sometimes, the signal distortion gets so worse that there is much misdetection. In addition, large leakage power in test generates lots of heat dissipation which may lower transistors' reliability, and even cause physical damage to transistors. Hence, in order to increase test reliability and lower negative effect on circuits under test, the leakage current should be well under control during test.

In current VDSM technology era, the researches on leakage current during test are in its gestation phase, and there are some leakage reduction techniques using low-power design methodologies[13,14]. One of the techniques is Input Vector Control — during standby mode the power management units drive the circuit inputs to a pre-computed MLV (minimum leakage vector)[15∼17]. Power Gating is a good way to reduce leakage current and dynamic power[18,19]. However, it is difficult to design the Power Gating because of

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This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant Nos. 60576031, 60633060, 60606008, 90607010, the National Grand Fundamental Research 973 Program of China under Grant Nos. 2005CB321604 and 2005CB321605, and the Science Foundation of Hefei University of Technology under Grant Nos. 070501F and 060501F. Y. Han's work is also supported by the fund of Chinese Academy of Sciences due to the President Scholarship.

a trade-off between area, power and performance. It also takes too much area overhead so that it is seldom used in practice. Other methodologies such as Threshold Voltage Control and Source Biasing could reduce IC's (integrated circuit) leakage current caused by sub-threshold leakage current to a certain extent, but it would lower performance as a sacrifice at the same time[6,20~22].

In this paper, using characteristics of test, we propose techniques based on don't care bits assignment to optimize the leakage current when combinational or sequential circuits are under test.

This paper is organized as follows. Section 2 describes the constituents of the leakage current, the transistor stacking effect and the leakage current simulator. Section 3 provides the optimization techniques which are based on don't care bits assignment using the genetic algorithm, and applies the techniques to combinational circuits and sequential circuits during test. In Section 4, we present simulation results of the techniques and compare them with related work. Finally, we conclude in Section 5.

2 Leakage Current Analysis and Estimation

2.1 Leakage Current Analysis

In order to effectually reduce leakage current during test, firstly we should estimate the leakage current which is composed of sub-threshold leakage current, gate-oxide leakage current and band-to-band-Tunneling leakage[23]. In current CMOS (Complementary Metal-Oxide-Semiconductor) technologies, the sub-threshold leakage current is much larger than other leakage current components. So we focus on estimating the sub-threshold current instead of the total leakage current. The sub-threshold current is the drain-source current of an OFF transistor and it can be calculated by the following equation[24]:

$$I_{\rm sub} = \mu_0 \frac{w_{\rm eff}}{L_{\rm eff}} v_{\rm T}^2 \sqrt{\frac{q\varepsilon_{\rm s} N_{\rm cheff}}{2\Phi_{\rm s}}} \Big(1 - e^{-\frac{V_{\rm ds}}{v_{\rm T}}}\Big) \cdot exp\Big[\frac{(V_{\rm gs} - V_{\rm T} - \gamma V_{\rm sb} + \eta V_{\rm ds})}{n v_{\rm T}}\Big] \qquad (1)$$

where μ_0 is the zero bias mobility and γ is the linear body effect coefficient. η is the drain-induced barrier lowering (DIBL) coefficient, representing the effect of $V_{\rm ds}$ on threshold voltage. Here, $L_{\rm eff}$, $W_{\rm eff}$ and $V_{\rm T}$ present the effective channel length, the effective width and the thermal voltage, respectively. For a small individual device, leakage current can be calculated by (1). But for a whole circuit, the leakage current cannot be computed by (1) because of the high time complexity etc. Therefore, how to estimate VLSI circuit's leakage current quickly and effectually is an important problem to be explored.

In fact, the stacking effect, which is caused by the transistor body effect, can have an impact on the sub-threshold current to a certain extent. Turning "OFF" more than one transistor in a stack of transistors forces the intermediate node voltage to go to a value higher than zero, which causes a negative $V_{\rm gs}$, negative $V_{\rm bs}$ (more body effect) and reduces $V_{\rm ds}$ (less DIBL) in the top transistor, thereby considerably decreasing the sub-threshold current flowing through the stack. This effect, known as the "stacking effect"[25], has been widely used to reduce the sub-threshold leakage in logic circuits. The current drawn by the logic block is dependent on the configuration of the ON and OFF transistors. The OFF transistors draw the leakage current while the ON transistors provide the conducting paths to the power supply nodes[26]. So the leakage current of a circuit depends on its input vectors combination, and we can reduce leakage current in CMOS VLSI circuits by input test vectors control.

2.2 Leakage Current Estimation

Most existing leakage estimation models are based on circuit level and have a high time complexity. Therefore, better leakage estimation method should be created in the advanced technology era[27].

Table 1. Leakage Current Values for Different Input Combinations of a 3-Input NAND Gate

3-Input NAND Gate		
Input Vector	Output	Leakage Current (pA)
0111	0	2599.40
110	1	155.50
101	1	158.77
011	1	173.35
001, ***100***, ***010***	1	31.4575
000	1	18.0386

Because of the stacking effect, the leakage of a circuit depends on its input vectors. Table 1 shows different leakage current values for all input combinations of a 3-input NAND gate. When the input combinations are ***001***, ***100*** and ***010***, they cause approximate values of leakage current. To simplify, we regard them as the same values. This phenomena caused by the stacking effect, also occurs in other kinds of logic gates. Based on the phenomena, a kind of leakage current simulator is built up to estimate the leakage current.

The following procedure describes how the simulator can be used to calculate the leakage current of a CMOS circuit during test.

1) Build the models of all kinds of logic gates using the BPTM (Berkeley Predictive Technology Model). Because it is seldom that logic gates have more than 10 inputs in CUT, we can simplify the problem. For example, we only consider from 2-input NAND gate to 10-input NAND gate.

2) Based on the phenomena, we use accurate switch level simulator (HSPICE) to investigate all currents of each cell under all input states. Then we set up leakage current tables for all types of basic gates.

3) Read in the netlist of CUT. Hence, the evaluation of average leakage current of a circuit only requires one pass of the circuit from the primary inputs to the primary outputs, calculating the state of each gate, and summing all leakage currents.

In this way, we can use the simulator to estimate the leakage current of a circuit under test quickly and effectually.

3 Leakage Current Optimization Using Don't Care Bits Assignment in Test Vectors

3.1 Don't Care Bits in Test Vectors

During test, test vectors are applied to the primary inputs of a circuit under test (CUT) firstly. After a functional period, test responses are captured from the primary outputs. Finally, test results are generated by the analysis on the test responses. This is the test process. In order to keep low test cost with high fault coverage, the test time should be minimized and the test vectors should be completed. So the switching activity of the circuit's internal nodes is higher during test. In the VDSM technology era, the different states of the internal nodes cause different leakage currents, which are already described in Section 2. Obviously, the test vectors influence the states of internal nodes and the test fault coverage.

In some test set generated by automatic test pattern generation (ATPG), a number of inputs do not need to be evaluated, which are applied by unspecified values. So the corresponding test vectors are composed of specified values (0 or 1) and unspecified values (don't care bits, X bits). The don't care bits are much more than the specified values to large scale IC. The X inputs can be set to either logic value 0 or 1 without losing fault coverage. In general, the don't care bits are assigned randomly in test. However, the random assignment may cause large leakage current and bring negative effect to the circuit during test.

In this paper, we propose techniques to reduce leakage current during test application. Firstly, we find the test set containing Xs which is generated by ATPG. Then through separately filling the Xs of test set produced by our leakage current simulator, the Xs are filled test vectors without losing fault coverage, we can get the minimum leakage vector (MLV) which causes minimum leakage current in circuit. Hence, by controlling the leakage current, the test power dissipation is reduced.

3.2 Leakage Optimization Algorithm for Combinational Circuits

To small scale integration, we can enumerate each valid assignment on don't care bits in order to get the optimal assignment causing minimum leakage current. However, to large scale integration, it is an NP-complete problem because there are too many don't care bits to find each valid assignment on them. Fortunately, some illumination algorithms could solve this problem.

A genetic algorithm (GA)[28] is a heuristic search algorithm for the solution of optimization problems. It starts from a random initial guess solution, and then better descendants are tried in an attempt to find the one that is the best under some criteria and conditions.

In the genetic algorithm in this paper, the population is a set of potential don't care bits assignments (the X can take either logic value 0 or 1). For example, an original test vector is ***1X0XX***, and the corresponding population contains ***10000***, ***10001***, ***10010***, ***10011***, ***11000***, ***11001*** etc. Each assignment represents one chromosome. After GA determines how fit each assignment is, some assignments are selected from the population to reproduce. The two selected chromosomes crossover and split again. Afterwards, the two new assignments mutate. Then the process is repeated a certain number of times until a good enough solution will be found. The following operations are defined for a population:

Fitness is a measure of how well the chromosome fits the search space, which in this paper is whether the assignment causes the minimum leakage current.

Selection is an operation of selecting the best genomes from the modified population for the next generation. The best genomes mean that the selected assignments are able to cause smaller leakage current.

Crossover is a process of exchanging a number of genes between two genomes of a population. The crossover occurs at random place in the chromosome. We hope that some reproduced chromosomes which are new assignments could cause smaller leakage current. For example, the chromosome ***10100*** when crossed with ***01000*** at the second bit produces the new chromosomes ***10000*** and ***01100***.

Mutation is an operation of randomly altering the chromosomes. For instance, the assignment ***10000*** mutates at the second bit and gives the new assignment ***11000***.

When a combinational circuit is under test, test vectors are applied to the primary inputs, as shown in Fig.1. The states of the internal nodes of the circuit change as soon as the new test vectors are applied in case of no delay in the circuit. We call the test vector a test vector slice (TVS) which is applied to the inputs in a clock period.

[27] presented a GA method to find the minimum leakage pattern. We use it with our simulator as follows. From GA, at first, we randomly assign the don't care bits in a TVS to generate the initial population. In the population, all vectors are the same except for the don't care bits. For example, there are two unspecified bits in the TVS ***1X1X0***. The initial population contains ***11110***, ***10100***, ***10110*** etc. Then, we use the simulator described in Section 2 to calculate the fitness of every assignments in the population. Two fit vectors which could cause smaller leakage current are selected out from the population and called them parents. By random crossover and random mutation, we get the produced vectors called children[27]. Afterwards, the children are put into a new set called the new generation. Then, we repeat the process a certain number of times so that we hope to get better don't care bits assignment of the TVS. This process is shown in Fig.2. Using the technique, we can find the assignments of all of the TVSs which compose the MLV. It means that the MLV has been specified (Fig.3).

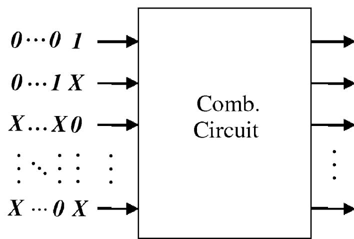


Fig.1. Test for combinational circuit.

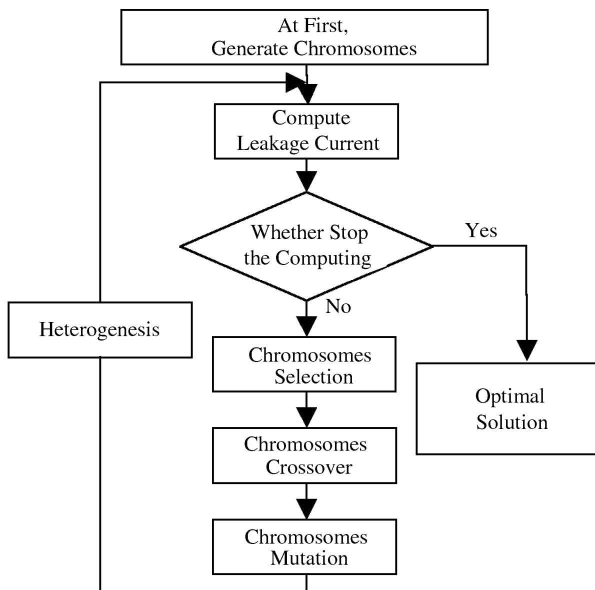
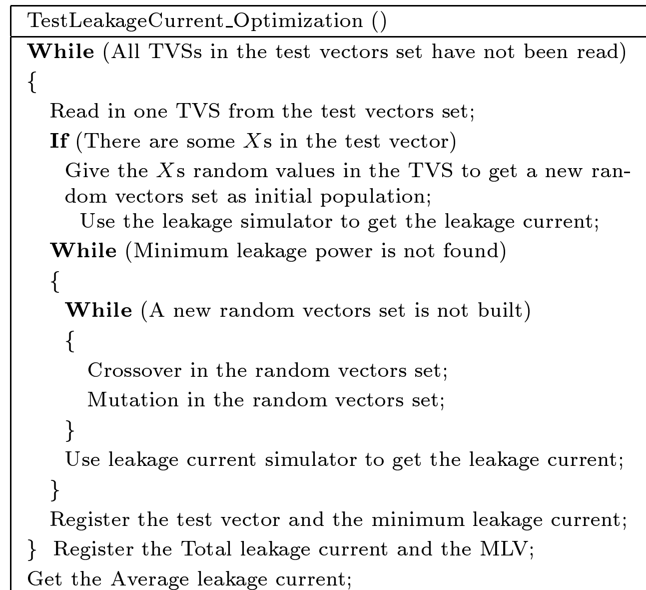


Fig.2. Flowchart of GA.

3.3 Leakage Optimization Algorithm for Sequential Circuits

Full scan is an effectual methodology in test and it is widely used for sequential circuits test. The leakage optimization algorithm is also fit for sequential circuits test. In full scan design, a sequential circuit is composed of a combinational circuit with added flip-flops as memory elements, and all of the flip-flops in a circuit are connected into serial chains. In this paper, to simplify the problem, we assume that there is only one chain in a circuit (Fig.4). Hence, all the flip-flops are configured as a chain in test mode. During test, part of a TVS is applied to the input of the scan chain. The input is named scan which is shown in Fig.3. In current technology era, there is the peak test power when the circuit is in the capture period. It is obvious that the peak test power includes dynamic power and leakage power. So, in this paper we aim at decreasing



```
TestLeakageCurrent_Optimization ()
While (All TVSs in the test vectors set have not been read)
{
  Read in one TVS from the test vectors set;
  If (There are some Xs in the test vector)
    Give the Xs random values in the TVS to get a new ran-
    dom vectors set as initial population;
      Use the leakage simulator to get the leakage current;
  While (Minimum leakage power is not found)
  {
    While (A new random vectors set is not built)
    {
       Crossover in the random vectors set;
       Mutation in the random vectors set;
    }
    Use leakage current simulator to get the leakage current;
  }
  Register the test vector and the minimum leakage current;
} Register the Total leakage current and the MLV;
Get the Average leakage current;
```

Fig.3. Optimization flow for finding minimum test leakage current.

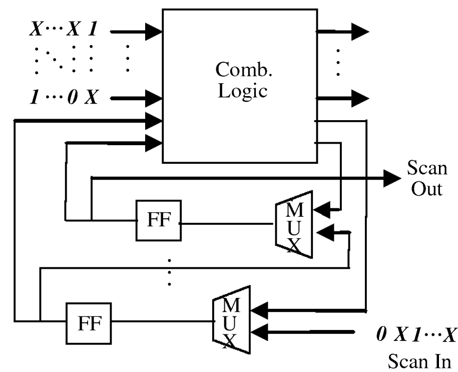


Fig.4. Test for sequential circuit.

leakage current at that time which is helpful to reduce the peak test power.

The test process on sequential circuits is similar to that on combinational circuits. The important difference is that part of TVS is directly applied to primary inputs of a combinational logic (PIs) while other bits are shifted into the two flip-flops as pseudo primary inputs (PPIs). Therefore, the optimization algorithm takes into account the PPIs.

In the same way, we can also find the maximum leakage current of combinational circuits and sequential circuits during test based on don't care bits assignment.

4 Experimental Results

We conducted experiments to evaluate the leakage current optimization techniques based on don't care bits assignments, using C++ under P4 3.0G (HT) CPU, 256MB SDRAM memory hardware platform. The target circuits include six ISCAS85 combinational circuits and seven ISCAS89 sequential circuits. We use BPTM 130nm technology[29] for all experiments, and also employ MINTEST test sets[30] all of which achieve 100% fault coverage.

At first, we use our leakage current optimization techniques on the selected combinational circuits. Simulation results are presented in Tables 2 and 3 below. These techniques using the GA are applied to optimize every TVS, so that we can specify the don't care bits to get the minimum and the maximum leakage currents corresponding to each slice. After that, we also get the MLV during test. The average minimum leakage current (*Avg. Min. Leakage*) is the average of the leakage currents caused by the TVSs of the MLV. In addition, the average maximum leakage current (*Avg. Max. Leakage*) is the average of the leakage currents produced by the TVSs of the maximum leakage vector which causes the maximum leakage current. They are all shown in the tables below. In order to increase the speed of GA to find MLV, we select some assignments, which could cause smaller leakage currents, from the random assignments of the don't care bits in a TVS as the initial population.

From Table 3, we see that the proposed techniques could quickly find the MLV, the minimum and the maximum leakage currents in large search space. (2) is used to evaluate the leakage power range in Table 2. The leakage power range is also the leakage current range. And the techniques decrease the leakage current by no more than 20% in 130nm technology of the selected combinational circuits. However, there is an exponential increase in leakage current with the development of process technology. It has been shown that the proportion of static power would exceed 42% in 90nm technology[31]. Therefore, the optimization techniques would have a better effect in deeper process.

$$\text{Leakage Power Range} = \frac{GA_Avg.Max. - GA_Avg.Min.}{GA_Avg.Min.} \times 100\%. \quad (2)$$

In addition, we assign the don't care bits randomly, and repeat the assignment 10 000 times to find the minimum leakage current and the maximum leakage current (as shown in Table 3). The effects of random assignment technique are evaluated by (3). It is seen that the random assignment technique is not good, be-

Table 2. Minimum and Maximum Leakage Optimization Results of Combinational Circuits in Test

Circuit	Gate Counts	Primary Inputs	X (%)	GA		Leakage Power Range (%)
				Avg. Min. Leakage (pA)	*Avg. Max. Leakage* (pA)	
C1355	625	41	4.34	358 274	358 509	0.07
C1908	830	33	23.28	647 514	660 085	1.94
C2670	1 459	233	77.49	1 029 095	1 186 583	15.30
C3540	1 613	50	53.35	1 444 529	1 484 509	2.77
C5315	2 813	178	66.17	1 964 515	2 230 912	13.56
C7552	3 685	207	57.11	2 900 997	3 022 674	4.19

Table 3. Comparison of the GA Method with the Random Assignment Method for Estimating the Minimum and Maximum Leakage of Combinational Circuits in Test

Circuit	GA				Random (do the simulation 10 000 times)			Leakage Power Reduction (%)
	Avg. Min. Leakage (pA)	Runtime (s)	*Avg. Max. Leakage* (pA)	Runtime (s)	*Avg. Min. Leakage* (pA)	*Avg. Max. Leakage* (pA)	Runtime (s)	
C1355	358 274	52.72	358 509	52.91	358 274	358 509	3 387.42	0.00
C1908	647 514	347.56	660 085	355.25	655 191	659 284	6 468.81	207.13
C2670	1 029 095	804.64	1 186 583	811.80	1 079 438	1 135 521	4 438.56	108.81
C3540	1 444 529	452.55	1 484 509	462.81	1 455 621	1 471 824	6 496.99	146.74
C5315	1 964 515	1 313.03	2 230 912	1 286.02	2 072 263	2 160 404	4 059.25	202.24
C7552	2 900 997	1 391.97	3 022 674	1 413.83	2 934 861	2 955 653	6 611.64	485.21

Table 4. Minimum and Maximum Leakage Optimization Results of Sequential Circuits in Test

Circuit	Gate Counts	Primary Inputs	DFFs	X (%)	GA		Leakage Power Range (%)
					Avg. Min. Leakage (pA)	*Avg. Max. Leakage* (pA)	
S641	107	35	19	49.36	260 466	281 056	7.91
S1196	388	14	18	56.45	388 117	441 567	13.77
S1238	428	14	18	56.80	387 596	440 238	13.58
S5378	1 004	35	179	72.62	1 269 451	1 503 277	18.42
S9234	2 027	36	211	73.00	3 685 433	4 400 217	19.39
S13207	2 573	62	638	93.15	5 030 023	6 192 659	23.11
S35932	12 204	35	1 728	35.30	12 057 921	14 056 783	16.58

Table 5. Comparison of the GA Method with the Random Assignment Method for Estimating the Minimum and Maximum Leakage of Sequential Circuits in Test

Circuit	GA				Random (do the simulation 10000 times)			Leakage Power Reduction (%)
	Avg. Min. Leakage (pA)	Runtime (s)	*Avg. Max. Leakage* (pA)	Runtime (s)	*Avg. Min. Leakage* (pA)	*Avg. Max. Leakage* (pA)	Runtime (s)	
S641	260 466	67.30	281 056	69.62	266 812	276 336	1 746.38	116.19
S1196	388 117	493.26	441 567	496.94	400 915	421 247	4 263.60	162.89
S1238	387 596	556.61	440 238	569.55	399 123	422 935	5 036.42	121.07
S5378	1 269 451	1 372.82	1 503 277	1 386.68	1 336 217	1 384 572	13 680.32	383.56
S9234	3 685 433	3 251.46	4 400 217	3 306.13	4 018 721	4 306 468	25 672.15	148.41
S13207	5 030 023	8 316.32	6 192 659	8 231.89	5 187 301	5 803 126	862 215.33	88.79
S35932	12 057 921	25 622.57	14 056 783	26 216.70	12 273 240	13 789 241	1 045 317.59	31.85

cause its optimization range is narrow and it spends an unaccepted time period. The GA method can reduce leakage power almost 5 times more than random method on C7552 circuit. Otherwise, because the don't care bits in the C1355 circuit are few, both of the two techniques cover the search space. Thus, they have the same effect on C1355.

$$\text{Leakage power reduction} = \frac{GA.Avg(Max.-Min.) \; - \; Random.Avg(Max.-Min.)}{Random.Avg(Max.-Min.)} \times 100\%. \quad (3)$$

Fig.5 shows the experimental results of C5315 circuit that an approximate linear increase of the leakage power range is proportional to the increase of amount of don't care bits. It means that we can use the proposed techniques to get smaller leakage current during test if ATPG is modified to produce more don't care bits. Here, the test vectors are produced by LFSR. The ratio of the don't care bits cannot be 100% because of the fault coverage.

Tables 4 and 5 show the experiments on seven ISCAS89 sequential circuits. In the experiments, it is supposed that there is only one scan chain in each circuit. Leakage power range in Table 4 is calculated by (2), and leakage power reduction in Table 5 is computed by (3). The two tables show that the proposed techniques also fit for the sequential circuits and it is better than the random assignment method. However, it is different that the effect of a PPI is not the same as that of a PI, so the leakage power range is not in proportion to the magnitude of the don't care bits. In addition, the PPIs are something like control points by which we can directly control the states of some internal nodes. By the control points, we can further optimize leakage current of some inside parts of circuits. Hence, the proposed techniques have a better effect on sequential circuits than on combinational circuits.

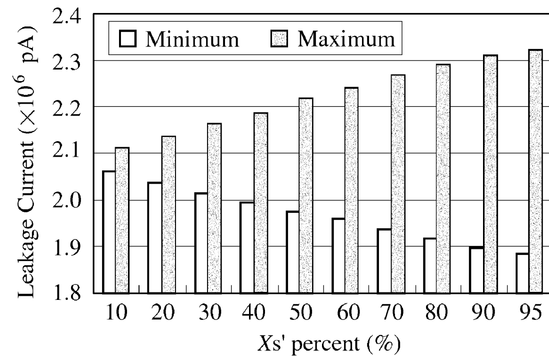


Fig.5. Effect of the proportion of don't care bits upon leakage current (C5315).

5 Conclusion

Because there are a lot of don't care bits in test vectors and they do not affect the test result whether they are set to 1 or 0. It is generally believed that don't care bits could only be assigned for test data compression to achieve high test data compression ratio. Nowadays, as we all know, test frequency is much lower than working frequency because of high test power. Test time is much prolonged and test cost is also increased. Thus, recently, don't care bits are often used

for low dynamic power test. In the future, high leakage test power would be an important problem which prevents us from increasing test frequency.

In this paper, we propose techniques to decrease power dissipation by leakage current reduction during test application. The techniques identify the don't care bits of each test vector. Then, it reassigns logic values to the X inputs in order to decrease the leakage current during test. Experimental results for benchmark circuits show that the proposed techniques can reduce the leakage currents of combinational circuits and sequential circuits during test without losing fault coverage. We apply the low leakage method in test area. In our techniques, genetic algorithm also can be replaced by other advanced greedy algorithms to get better results. Our techniques are easy to realize and could be embedded in other low power test methods or other test data compression methods. Due to the rising leadage current with the scaling down of the integrated circuits, the proposed techniques provide a very attractive scheme to reduce leakage power during IC test.

Acknowledgements We would like to thank Mrs. Hua-Wei Li, Mr. Yong-Jun Xue and Mr. Ge Zhang for useful discussions. We acknowledge the support of Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences, and other members of the key laboratory.

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