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# What's Missing in Agile Hardware Design? Verification!

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Agile hardware design is an approach to developing hardware systems that draws inspiration from the principles and practices of agile software development. It emphasizes collaboration, flexibility, iterative development, and quick adaptation to changing requirements. In agile hardware design, the focus is on delivering functional hardware systems in shorter development cycles while maintaining high-quality and customer satisfaction.

In particular, agile hardware design is of great interest in the open-source hardware community. Open-source hardware development —such as RISC-V— is at the forefront of initiatives to democratize hardware and drive innovation in chip design forward. Agile design is instrumental for the RISC-V community because it supports rapid iteration, accommodates the evolving RISC-V standard and the addition of custom extensions, improves community collaboration and time-to-market, and addresses the design challenges associated with complex architectural features.

Among significant innovations based on agile hardware design is the recently announced XiangShan RISC-V core which is currently the highest performing RISC-V out-of-order microprocessor core with single-thread performance exceeding both existing RISC-V cores and a state-of-the-art ARM core, Cortex-A76. The creators of this platform have published their agile design methodology in a flagship computer architecture venue, MICRO, with a paper that has been selected through peer review to be among the best dozen papers in all of computer architecture in one year for publication in IEEE Micro Top Picks.

A key contributor to this breakthrough has been integrating hardware verification into the agile methodology. Hardware verification is crucial in designing digital platforms, as it ensures that semiconductor chips operate correctly and reliably according to the architecture specifications. Verification guarantees compliance with standards, and helps detect and rectify design errors, validate system-level functionality, optimize performance and power consumption, and enhance hardware reliability and safety. It plays a fundamental role in creating robust and dependable CPUs that meet the requirements of various applications and workloads.

There are also a number of trends in recent years that have made robust verification indispensable to hardware design and deployment. These include the slowdown in Moore's Law resulting in more heterogeneity and diversity in design, concerns about security and integrity in digital platforms, and the emergence of open-source hardware (e.g., RISC-V) which is anchored on collaboration among a large community of developers without centralized ownership and coordination. Therefore, contributions to integrating verification into agile design are not only of important to the RISC-V community but also of great interest to the broader hardware design industry.

This paper titled "Functional Verification for Agile RISC-V Processor Development" identifies a key limitation in the collaboration and information exchange between existing agile hardware design methodologies and conventional functional verification. This disconnect hinders the seamless integration of verification workflows and toolchains with agile development practices. The authors address this issue by proposing workflow integration that incorporates collaborative task delegation and dynamic information exchange as fundamental principles for achieving agile hardware design with functional verification.

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Perspective

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The authors demonstrate the efficacy of their approach by presenting an RISC-V core design within the integrated agile design and verification framework. Through their evaluation, they showcase how functional bugs can be detected and resolved using the approach. It is important to note that these tools and methodologies are not merely conceptual ideas or prototypes but are practical toolchains that have been tested and applied to real-world designs, such as XIANGSHAN. The latter underscores their relevance and applicability in both academic and industrial settings.

**Babak Falsafi** is a professor in the School of Computer and Communication Sciences and the founder of EcoCloud, an industrial/academic consortium at EPFL investigating scalable sustainable information technology. He has made numerous contributions to computer system design and evaluation including a scalable multiprocessor architecture which was prototyped by Sun Microsystems (now Oracle), snoop filters incorporated into multi-socket x86 servers and IBM BlueGene supercomputers, spatial and temporal memory streaming that appear in ARM cores, and computer system performance evaluation methodologies that have been in use by AMD, HP and Google PerfKit . He has shown that hardware memory consistency models are neither necessary (in the 90's) nor sufficient (a decade later) to achieve high performance in servers. These results eventually led to fence speculation in modern CPUs. His work on cloud-native CPUs laid the foundation for the first generation of Cavium ARM server CPUs, ThunderX. He is a recipient of an NSF CAREER award, IBM Faculty Partnership Awards, and an Alfred P. Sloan Research Fellowship. He is a fellow of ACM and IEEE.